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TITLE: INTEGRATED CIRCUIT PACKAGE HAVING ENHANCED HEAT
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ABSTRACT:

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providing for improved power dissipation in the plastic packaged IC (40).

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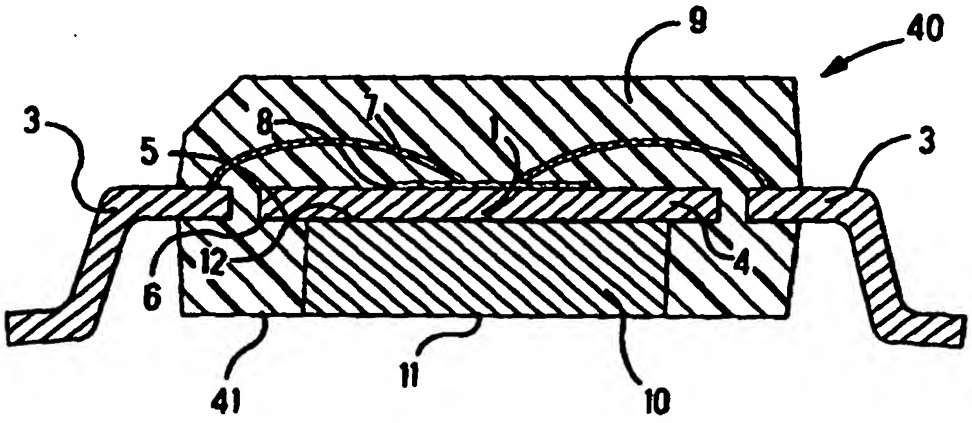

(57) Abstract

A plastic package integrated circuit (40) has a heat sink structure with a major surface (11) exposed on a seating plane side (41) of the packaged IC. A puck (10) is attached to a die attach paddle (4) of a lead frame (2). The puck (10) is also electrically attached to a ground point of the IC die (1). The puck (10) comprises a thermally conductive first material combined with a thermal expansion constraining second material providing for improved power dissipation in the plastic packaged IC (40).

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INTEGRATED CIRCUIT PACKAGE HAVING ENHANCED HEAT DISSIPATION AND GROUNDING

Background of the Invention

The advent of plastic packaging for digital integrated circuits (ICs) has led to substantial reductions in cost for ICs and the products into which they are incorporated. The demand by the industry for high volume and low cost has led to a high degree of mechanization in the manufacture of ICs. The electronics industry standardizes on a limited number of package sizes and shapes as new packages are introduced giving rise to manufacturing advantages such as economies of scale and optimization of the manufacturing processes for high volume and high yield. Advantageously, a specific IC package may be used for different types of IC dies. Therefore, specialized and low volume ICs can realize the benefits of low cost standardized packaging under some circumstances. The printed circuit board (PCB) manufacturing processes are designed and optimized to accept the standard package sizes and shapes available from IC manufacturers.

As digital ICs become faster and more highly integrated, they consume and, therefore, must dissipate increasing amounts of power during operation. For some ICs, it is possible to dissipate all of the generated heat through the wirebonds, the lead frame and the leads to the PCB. For ICs that have relatively higher power dissipation requirements, it is known to attach a metal puck on the top of a lead frame. The puck is attached to the lead frame by attachment compound or by brazing

as disclosed in U.S. Patent No. 3,930,114. The puck is disposed within a plastic IC package so that an major surface of the puck is exposed on a top side of the IC, the top side being the side facing away from the IC leads that engage a PCB. In some cases, metal fins are attached to the puck for additional heat dissipating capacity. Heat generated by the IC flows from the die and/or the lead frame through the attachment compound and to the puck and/or fins. Air flows or is forced over the puck surface/fins for cooling to dissipate the heat generated by the IC. As miniaturization and communication capability progresses, however, the smaller packaging provides for less air volume for cooling in higher power products. There is a need, therefore, for a small plastic package for power ICs having an efficient heat dissipation capability.

The plastic packages that are conventional in the industry are advantageously an acceptable low cost packaging option for most digital and low frequency ICs. In the interest of miniaturization, light weight, and low cost for emerging mobile communication applications, plastic packaging is an attractive option. Many of the components in mobile communication applications require operation at radio frequencies(RF) and higher. The conventional plastic IC packaging, however, has certain disadvantages at RF and microwave operating frequencies.

Important challenges in packaging an RF component are realization of a high quality conductive path to RF ground and heat dissipation for active components such as amplifiers. In the case of a standard plastic package, the path to RF ground would typically flow from

the die, through a wire and wirebond to the leads and then to a reference point on the PCB. The plastic of the package is a dielectric and surrounds the electrical paths. This produces resistive, inductive, and capacitive parasitics in the path to RF ground that adversely affect the frequency response of the packaged component. The value of the parasitic vary due to manufacturing irregularities in the process for molding the plastic package. Accordingly, the uncontrolled parasitics are unpredictable which cause unacceptable variations in the operating performance of the parts.

It is known to improve the quality of an RF ground in a plastic package for a high frequency component by utilizing multiple leads in a single package for a path to RF ground. Adjacent leads that would be singulated in a conventional low frequency IC package are joined as one or more large lead. The large lead visually resembles a "bat wing" as opposed to the conventional "gull wing" and the package is colloquially termed the "bat wing" package. The "bat wing" package has lower parasitics in the path to RF ground, but disadvantageously, requires a larger package size to provide the necessary number and type of leads. The larger package is in contravention of the effort to miniaturize components and the products into which they are incorporated.

It is an object of the present invention to provide a light weight and low cost plastic package for a high frequency integrated circuit or device.

It is an object of the present invention to provide a high quality RF ground in an IC package.

It is an object of the present invention to provide a small IC package suitable for RF components capable of dissipating more heat that conventional packages of similar size.

An integrated circuit package having a seating plane side comprises a die, a lead frame, and a metal puck disposed on said lead frame. The lead frame is encased in the package material exposing a surface of the puck and the leads. The surface of the puck is exposed on the seating plane side of the integrated circuit package.

It is an advantage of the present invention that a package for a high frequency IC has a high quality path to RF ground.

It is an advantage of the present invention that a package for a high frequency IC can dissipate substantial heat in a relatively small package and with limited air volume.

It is an advantage of the present invention that an IC package suitable for high frequency components is compatible with conventional low cost, high volume digital IC packaging processes.

It is an advantage of the present invention that an IC package suitable for high frequency components is compatible with known PCB manufacturing processes.

It is an advantage of the present invention that a dissipation material is constrained from thermal expansion by a constraining material sufficient so as to

reduce stress on the die so as not to exceed the tensile strength of the die.

It is an advantage of the present invention that a material can have an engineered coefficient of thermal expansion providing for a match to an IC die, while still providing favorable high thermal conductivity and dissipation.

Embodiments of the invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 is a cross sectional view of a plastic integrated circuit package according to the teachings of the present invention.

Figure 2 is a cross sectional view of an alternate embodiment of a plastic integrated circuit package according to the teachings of the present invention showing coplanarity between ends of the integrated circuit package leads distal from the die attach paddle and an exposed first major surface of the puck.

Figure 3 is a cross sectional view of an alternate embodiment of a plastic integrated circuit package according to the teachings of the present invention showing coplanarity between ends of the integrated circuit package leads and the bottom surface of the puck.

Figure 4 is a plan view of a position in a dual position lead frame strip for use in a preferred embodiment according to the teachings of the present invention as seen prior to encapsulation and

singulation. The IC package body outline is shown in phantom line.

Figure 5 is a plan view of a position in a dual position strip of an alternate embodiment of a lead frame strip according to the teachings of the present invention.

Figure 6 is a plan view of a position in a dual position puck frame strip illustrating two pucks prior to attachment to a lead frame and singulation. The puck frame is for use in conjunction with the lead frame illustrated in Figures 4 and 5 to manufacture an integrated circuit package according to the teachings of the present invention.

Figure 7 is a cross sectional view of the puck cut along the lines 7--7 of Figure 6.

Figure 8 is a view of a die with wire bonds attached to the die attach paddle according to the teachings of the present invention.

Figure 9 is a perspective view of the puck frame superimposed upon the lead frame after metallurgical attachment according to the teachings of the present invention and prior to die attach, encapsulation, and singulation. The superimposition of the lead frame and puck frame shows conceptual alignment of the two frames.

Figure 10 is a perspective view of a plastic packaged integrated circuit shown with the plastic package partially cut away to illustrate the relative positioning of the die, the lead frame, the puck, and the leads according to the teachings of the present invention.

Figure 11 is a cross sectional view of a punch press and puck frame prior to singulation of the pucks.

Figure 12 is a cross sectional view of a punch press and puck frame subsequent to singulation of the pucks.

Figure 13 is a cross sectional view of an adapter that retains the pucks and fixture for receipt of prepared lead frames.

Figure 14 is a cross sectional view of the adapter assembly held by a transfer tool.

Figure 15 is a cross sectional view of the adapter and pucks placed over a lead frame fixture and lead frame.

Figure 16 is a cross sectional view of the adapter and pucks over a lead frame fixture with cover plate and weight prior to a reflow operation to attach the pucks to the lead frames.

Figure 17 is a perspective view of a plastic packaged integrated circuit shown with the plastic package partially cut away to illustrate the relative position of the seating plane side of the IC relative to the puck.

Figure 18 is a cross section of one embodiment of a puck according to the teaching of the present invention illustrating the different material layers of the puck.

With specific reference to Figures 1 through 10 of the drawings, an integrated circuit (IC) package **40** according to the teachings of the present invention has a seating plane side **41**. The seating plane side 41 is defined as that side of the IC toward which respective

ends of the leads, distal from the package, extend. In a preferred embodiment according to the teachings of the present invention, the IC package 40 is an SOIC-8 package according to the JEDEC standard 95, MS-012. When disposed on a printed circuit board, the seating plane side 41 is juxtaposed to or, in the case of surface mount IC packages, engages the printed circuit board substrate. The IC package 40 comprises an integrated circuit die 1 attached to a die attach paddle 4 of a lead frame 2 using electrically conductive adhesive 8. In a preferred embodiment, the IC die 1 is a GaAs based power amplifier, although any IC that may benefit from a high quality ground and efficient thermal dissipation capacity is appropriate. As can be appreciated by one of ordinary skill in the arts, a high frequency power amplifier requires heat dissipation capability as well as a high quality reference, or ground, for the high frequency energy. The die attach paddle 4 has a first side 5 on which the die is disposed and a second opposite side 6 on which is disposed a puck 10. The puck 10 is a solid copper cylindrical disc stamped out of metal having internal and external major surfaces 12,11. The internal major surface 12 of the puck 10 is electrically connected to the die attach paddle 4 by means such as soldering, brazing, or welding. A diameter of the puck 10 is sized relative to the die attach paddle 4 so as to fit within the confines of, but substantially cover the paddle 4. The integrated circuit die 1 has contacts 42 electrically attached to signal lines on the IC. The contacts 42 are electrically attached to respective leads 3 of the lead

frame 2 through a wire bond 7 using conventional means. Ground lines of the integrated circuit die 1 are electrically attached to the die attach paddle 4 through a wire bond 7 as illustrated in Figure 8. The integrated circuit package 40 is manufactured and the IC die 1 and puck 10 appropriately positioned so that the external major surface 11 of the puck is exposed after plastic packaging material 9 is formed around the die, lead frame, wirebonds, and puck. The external major surface 11 of the puck 10, which is the exposed surface 11 after encapsulation, is located on the seating plane side 41 of the IC package 40. For attachment of the IC package 40 to a printed circuit board, the leads 3 and the exposed surface 11 of the puck 10 are soldered to conductive traces on the printed circuit board substrate in a conventional manner. The printed circuit board is laid out to have a connection point to RF ground, or in an alternate embodiment, any ground, at a point between and central to the two parallel lines of connection points that receive the IC leads 3. The puck 10 is electrically attached to a ground trace or ground plane on the printed circuit board underneath the IC package. Soldering the exposed surface of the puck 10 to an electrical reference point on the PCB completes the electrical path from a point on the IC to the PCB. The conventional ground path is from the die through a wire bond to the lead of the lead frame, and the lead to the ground connection on the PCB. By virtue of the greater conductive cross sectional area through the conductive puck 10 as compared to the conductive cross sectional area of conventional IC leads or fused leads, there is a

lower inductive path from the IC to the PCB through the puck 10 than through the leads 3 as in the conventional manner. A lower inductive electrical path is particularly advantageous for a high frequency ground path. As may be appreciated by one of ordinary skill in the art, according to the teachings of the present invention, a high quality ground path is realized without increasing the size of the package. In some cases, it is advantageous to have one or more leads 3 of the packaged IC connected to the RF ground. A specific example might be if circuitry external to the packaged IC needed access to the reference or ground of the IC. In that case, a wire bond 7 could connect a ground contact 42 to the die attach paddle 4 as well as one or more leads 3 as desired. Alternatively, the lead frame 2 could be manufactured to have one or more leads 3 fused to the die attach paddle 4. See Figure 5 showing two of the leads 3 fused to the die attach paddle 4. Alternatively, provided that the IC die itself had a via through which a ground connection could be made, electrical connection to the die attach paddle 4 would not be through a wire bond 7, but rather through the IC die itself.

Attachment of the puck 10 in this manner also provides efficient thermal conduction from the IC die 1, through the die attach paddle 4, and through the puck 10, where heat is dissipated through the printed circuit board, ground traces, and/or a ground plane thereon. A thermal ground connection through the puck 10 is a more direct path and has a greater cross sectional area than an IC lead through which to conduct heat. Heat is

conducted through the puck 10 to a PCB by physical contact where is it further conducted through the PCB itself. The PCB has a larger surface area than the IC. As the heat is distributed over the larger surface area, it can be more efficiently dissipated.

With specific reference to Figure 9, a preferred process to manufacture a plastic packaged integrated circuit according to the teachings of the present invention comprises the steps of: attaching a puck 10 to a lead frame 2, attaching an integrated circuit die 1 to the lead frame 1, wire bonding electrical connections from the integrated circuit to a die attach paddle 4 of the lead frame 2 and to respective leads 3 of the lead frame 2, encapsulating the lead frame 2 with plastic packaging 9, trimming the packaged IC from the lead frame 2, and forming the leads 3 of the lead frame 2 into a finished part.

A preferred embodiment of the step of attaching a puck 10 to a lead frame 2 further comprises the steps of preparing the lead frame 2 by stenciling solder paste onto an unplated side of the lead frame 2. Solder paste is placed on the die attach paddle 4 of respective lead frames 2 in a strip. The prepared lead frame 3 is placed solder side up into a lead frame fixture 13 that holds the lead frame 2 stationary.

With specific reference to Figures 4 through 6 and 11 through 16 of the drawings, a puck frame 15 is placed onto registration pins (not shown) on punch tooling. The registration pins cooperate with registration holes 14 in the puck frame 15. The pucks 10 are singulated from a puck frame 15 by the punch tooling prior to

placement and attachment to the lead frame 2. There are registration holes 14 in the lead frame 2 that postionally coincide with the registration holes 14 in the puck frame 15. Figure 9 of the drawings illustrates the conceptual alignment of the puck frame 15 to the lead frame 2 showing coincidence of the registration holes 14 of the lead frame 2 and the puck frame 15 for proper alignment. Singulation comprises placing the puck frame 15 on a punch press **16**. When the punch press 16 is actuated, the pucks 10 are singulated and separated from the puck frame 15. The puck frame 15 remains on the punch press tooling 16. An adapter **17** is placed over the singulated pucks 10. The adapter 17 has guide holes **21**. A transfer tool **18** picks up the adapter 17 by vacuum actuation which holds the adapter 17 and the pucks 10 in proper position. The transfer tool 18 picks and places the adapter 17 and pucks 10 over the prepared lead frame 2 located on the lead frame fixture 13. Guide pins **22** of the lead frame fixture 13 cooperate with the guide holes 21 of the adapter to properly register the singulated pucks 10 to the lead frames 2. A cover plate **19** is placed over the adapter 17. The cover plate 19 is further covered by a weight **20**. The weighted lead frame fixture 13 assembly is heated in a controlled inert gas atmosphere to reflow the solder and attach the pucks 10 to respective lead frames 2. The prepared lead frame 2 with the pucks 10 thereon, is then used in the die attach, wire bonding, and encapsulation steps. The packaging steps using a lead frame 2 prepared with pucks 10 according to the teachings of the present invention result in a plastic

IC package having the external major surface of the puck 10 exposed on a seating plane side 41 of the finished IC package 40. It is preferred that the encapsulated lead frame 2 is trimmed and formed so the end of respective leads 3 distal from the lead frame 2 are substantially coplanar with the exposed surface 11 of the puck 10. The coplanarity provides for easier attachment of the puck 10 to the printed circuit substrate during the solder step of attaching leads to the printed circuit substrate. In one embodiment, the exposed surface 11 of the puck 10 is substantially coplanar with the seating plane side surface of the plastic of the IC as well as ends of the leads 3 distal from the lead frame 2. See Figure 2 of the drawings. In that case, a conventional trim and form tool is modified to form the ends of the leads 3 distal from the lead frame 2 to be coplanar with a seating plane side of the plastic package and puck 10. In an alternate embodiment, a thickness of the puck 10 is selected, so that the exposed surface protrudes from the seating plane side 41 of the packaged IC 40 a distance of approximately 5 mils for an SOIC-8 plastic package. The protrusion achieves the desired substantial coplanarity of ends of the leads and the exposed surface 11 of the puck 10 without a modification of the conventional trim and form tool. See Figure 3 of the drawings.

A solid copper puck 10 as disclosed hereinbefore is capable of dissipating heat in a plastic package for a four watt GaAs integrated circuit power device. The four watt device limitation is due in part to the thermal expansion differential between the die attach

paddle 4, the IC die 1, and the bonds therebetween. As the IC die 1 heats, heat transfers as intended to the die attach paddle 4 and puck 10. The die attach paddle 4, therefore, heats as does the IC die 1. Due to the different coefficients of thermal expansion between the GaAs IC die 1 and copper die attach paddle 4, a stress is imposed on the die 1. If the resulting stress exceeds the strength of the die 1, the die 1 cracks resulting in catastrophic device failure. The difference in thermal expansion coefficients between the die 1 and the die attach paddle 4 may be addressed in part through use of conductive adhesive to attach the die 1 to the die attach paddle 4. The compliance of the conductive adhesive relieves the stress between the die 1 and the die attach paddle 4 through resilient deformation. Disadvantageously, the conductive adhesive is less thermally conductive than less compliant methods of attachment. The lower thermal conductivity adversely affects the amount of heat that can be reliably dissipated through the puck 10, thereby limiting the overall power rating of the packaged IC 40. The general trend in the industry is toward higher power devices. There is a need, therefore, for a low cost plastic package that can dissipate heat for higher power devices with acceptable reliability.

In order to overcome these disadvantages, there is a need for a material from which a puck 10 can be made that exhibits high thermal conductivity while at the same time having a coefficient of thermal expansion matched to that of the IC die 1. In a package according to the teachings of the present invention wherein, a

material from which the puck 10 is made exhibits the desired thermal conductivity and coefficient of thermal expansion, the puck 10 is attached to the copper die attach paddle 4. The copper die attach paddle 4 has an opening 44 therein within which the die 1 is received. The internal major surface 12 of the puck 10 is larger than the opening 44 in the die attach paddle 4. By virtue of attachment of the puck 10 to the die attach paddle 4, a portion of the internal major surface 12 of the puck 10 provides a surface upon which the die 1 is received. The die 1 is soldered directly onto the internal major surface 12 of the puck 10 providing for a highly thermally and electrically conductive rigid bond between the die 1 and the puck 10. The puck 10, when made according to the teachings of the present invention exhibits thermal expansion within acceptable expansion limits of the IC die 1, thereby obviating the need for a compliant bond between the die 1 and the puck 10. It is the salient characteristics of the puck 10 that are matched to the IC die 1 that provides the intended advantage. The term "matched" is defined as significantly close so that within the anticipated range of operating temperature, the die 1 and the puck 10 exhibit similar thermal expansion so that the stress placed on the IC die 1 due to the respective expansions between the die 1 and the puck 10 does not exceed the tensile strength of the IC die 1. To further complicate matters, some IC dies 1, for example gallium arsenide, have a non linear coefficient of thermal expansion that decreases as the die temperature increases. The coefficient of thermal expansion, therefore, must be

carefully chosen so that the stress placed on the IC die 1 falls within an appropriate range. The carefully chosen material exhibiting the thermal expansion properties matched to the IC die 1 makes possible the direct attachment of die 1 to puck 10. The puck 10 is attached to the die attach paddle 4 by any known means including soldering, braising, welding or adhesive attachment. In a preferred embodiment of a packaged IC according to the teachings of the present invention, the die attach paddle 4 has an opening sufficiently large to fully receive the IC die 1. The IC die 1 is attached directly to the puck 10, by soldering for example, and is surrounded by the die attach paddle 4.

In one embodiment of a puck material according to the teaching of the present invention, the puck 10 is made from a laminated metal. The laminate comprises alternating thermal dissipation and constraining layers 30, 31. Conceptually, the dissipation layer is made from a high electrical and thermal conductivity material, typically metal. The constraining layer 31 provides acceptable and sufficient electrical and thermal conductivity but has a lower coefficient of expansion. The thermal dissipation layer 30 provides for the thermal and electrical conduction necessary for appropriate performance of the puck 10. The constraining layer 31, may have a lower but sufficient thermal and electrical thermal conductivity but due to its lower coefficient of thermal expansion limits or constrains the actual expansion of the thermal dissipation layer. The lamination of the two metals is performed according to conventional practice. The bond

between the thermal dissipation layer 30 and the constraining layer 31 is sufficiently strong to withstand the stress present at the interface of the two metals. Any odd number of layers is appropriate with the constraining layers being internal to the puck 10. The outside layers 33 having the higher thermal conductivity are attached to the PCB and the die 1/die attach paddle 4 respectively.

The properties of the laminated puck material may be selected by the selection of layer thicknesses and materials employed for the layers. Thermal conductivity and coefficient of thermal expansion is estimated from the following relations. For layered metal puck structures, the effective thermal conductivity, $k_{EFFECTIVE}$, is predicted using the following relation:

$$k_{EFFECTIVE} = \sum_i k_i \left(\frac{t}{t_i} \right)$$

where t is the total thickness of the puck 10, t_i is the layer thickness, k_i is the thermal conductivity of the layer, and i represents the number of layers. A simplified relation is used to predict the effective coefficient of thermal conductivity, $\alpha_{EFFECTIVE}$:

$$\alpha_{EFFECTIVE} = \frac{\sum_i \alpha_i t_i E_i}{\sum_i t_i E_i}$$

where t_i is the layer thickness , E_i is Young's Modulus of the layer, α_i is the coefficient of thermal expansion of the layer, and i represents the number of layers.

Accordingly, the effective values of thermal conductivity and coefficient of thermal expansion may be engineered through the selection of desired thicknesses of the conductive and constraining layers.

In an embodiment optimized for use with the GaAS IC die 1 using a power fabrication process the preferred puck material has nine layers, comprising five copper dissipation layers 30 each having a thickness of approximately 3 mils and four molybdenum, constraining layers 31, each having a thickness of approximately 3 mils. The laminated metal may be stamped and processed into a plastic package in identical fashion as with the solid copper puck as is described above.

In an alternate and preferred embodiment of a puck 10 according to the teaching to the present invention, the puck 10 is made from a mixture of two powered materials, typically metal comprising a dissipation material and a constraining material. Conceptually, the puck 10 made from powdered metal operates the same way the laminate version does, except that one layer is not constraining an adjacent layer, rather the material itself based on its heterogeneous composition, is constrained in X,Y and Z axes as opposed to along a plane (i.e. just the X and Y directions). The powdered materials are mixed in specific proportion, pressed, and sintered to an effective density of between 92 and 99 percent solid according to conventional practice. Although most metals are appropriate, depending upon the desired characteristics, the preferred dissipation material is copper and the preferred constraining material is tungsten.

The composition of the puck 10 is determined by employing conventional powder metallurgy techniques to obtain high thermal conductivity with the desired coefficient of thermal expansion. The theoretical density $\rho_{THEORETICAL}$, of a powdered metal material can be estimated by the following equation:

$$\rho_{THEORETICAL} = (Wt\%_{COPPER} \times \rho_{COPPER}) + (Wt\%_{TUNGSTEN} \times \rho_{TUNGSTEN})$$

where Wt% represents the percentage of the total weight of each material.

The nature of powdered metal materials is that in practice this theoretical density is never achieved due to processing variations. Therefore it is valuable to consider the powdered metal material in terms of its fractional density, the ratio of measured versus theoretical densities. This fractional density is an important component in determining final mechanical properties.

$$\rho_{FRACTIONAL} = \frac{\rho_{MEASURED}}{\rho_{THEORETICAL}}$$

For powder metal compositions of copper and tungsten, fractional densities of 86 to 96 % can be produced routinely. From known sample compositions of copper and tungsten powders, the properties of thermal conductivity and coefficient of thermal expansion have been known to follow empirical relationships similar to that for the theoretical density. The coefficient of thermal expansion, Cte, can be predicted using the following relation:

$$Cte_{PREDICTED} = \left[(Wt\%_{COPPER} \times Cte_{COPPER}) + (Wt\%_{TUNGSTEN} \times Cte_{TUNGSTEN})\right] \times n$$

Predicted values for the thermal conductivity, $k_{PREDICTED}$, are made using the following relation:

$$k_{PREDICTED} = \left[(Wt\%_{COPPER} \times k_{COPPER}) + (Wt\%_{TUNGSTEN} \times k_{TUNGSTEN})\right] \times (1/n)$$

where n is a factor associated with the density and structure of the powder metal compact. Values for n are in the range of 0.8 to 1.10. In many instances n can be approximated as:

$$n \approx \rho_{FRACTIONAL}$$

Through the use of these relationships to select the weight fraction of copper and tungsten, it is possible to simultaneously optimize the values for thermal conductivity and coefficient of thermal expansion to suit the mechanical and thermal characteristics of the integrated circuit die.

In a preferred embodiment of the puck 10 for a gallium arsenide IC die 1, the puck 10 is made using 10% by weight of copper and 90% by weight of tungsten pressed and sintered to yield a 94% solid puck weight.

As can be appreciated by one with ordinary skill in the art, the pressed and sintered puck 10 results in a final puck format rather than a sheet of metal that may be stamped. Therefore, the process by which the puck 10 would be attached to the die attach paddle 4 does not include a puck frame 15. Attachment of the puck 10 to the die attach paddle 4 is by way of a fixture to position the puck 10 over the lead frame. The puck 10

may thereafter be attached to the die attach paddle 4 of the lead frame 2. Solder is the preferred method of attachment of the puck 10 to the die 1.

Advantageously, both embodiments are capable of dissipating power for a 10 watt GaAs device in a reliable plastic package.

Other advantages of the invention are apparent from the detailed description by way of example, and from the accompanying drawings, and from the spirit and scope of the appended claims.

Claims:

1. A packaged integrated circuit having a seating plane side, the packaged integrated circuit comprising a die, a lead frame having a plurality of leads, and a conductive puck disposed on said lead frame, wherein said puck further comprises internal and external major surfaces, wherein said internal major surface engages said lead frame the lead frame being encased in a package exposing a surface of the puck and exposing said leads characterized in that:

said puck is exposed on a seating plane side of said encased lead frame.

2. A packaged integrated circuit as recited in claim 1, said lead frame further comprising a die attach paddle on which said die is disposed, said die having at least one contact wherein said contact is electrically connected to said puck.

3. A packaged integrated circuit as recited in claim 1 or 2 disposed on a printed circuit substrate having a ground connection point encased lead frame and wherein said external major surface of said puck is electrically connected to said ground connection point.

4. A packaged integrated circuit as recited in claim 1, 2 or 3 each said lead having an end distal from said lead frame which is substantially coplanar with said external major surface of said puck.

5. A packaged integrated circuit as recited in claim 1, 2, 3 or 4, wherein said external major surface of said puck is substantially coplanar with a seating plane side of said package.

6. A packaged integrated circuit as recited in claims 1, 2, 3, 4 or 5 wherein said puck comprises a thermally conductive first material combined with a thermal expansion constraining second material

7. A packaged integrated circuit as recited in claim 1, 2, 3, 4 or 5 wherein, said puck comprises at least one thermally conductive dissipation layer having a first coefficient of thermal expansion laminated to a constraining layer having a second coefficient of thermal expansion, said second coefficient of thermal expansion being less than said first coefficient of thermal expansion.

8. A packaged integrated circuit as recited in claim 7 wherein said puck comprises a plurality of alternating dissipation and constraining layers.

9. A packaged integrated circuit as recited in claim 7 or 8 wherein a total number of said dissipation and constraining layers is an odd quantity resulting in two outer layers.

10. A packaged integrated circuit as recited in claim 9 wherein each of said outer layers comprises one of said dissipation layers.

11. A packaged integrated circuit as recited in claims 7, 8, 9, or 10 wherein said dissipation layer comprises copper and said constraining layer comprises molybdenum.

12. A packaged integrated circuit as recited in claim 1 or 2 wherein said puck comprises at least one powdered thermally conductive dissipation material having a first coefficient of thermal expansion and a powdered constraining material having a second coefficient of thermal expansion wherein said second coefficient of thermal expansion is less than said first coefficient of thermal expansion.

13. A packaged integrated circuit as recited in claim 12 wherein said puck comprises 10-20% by weight of copper and 80-90% by weight of tungsten.

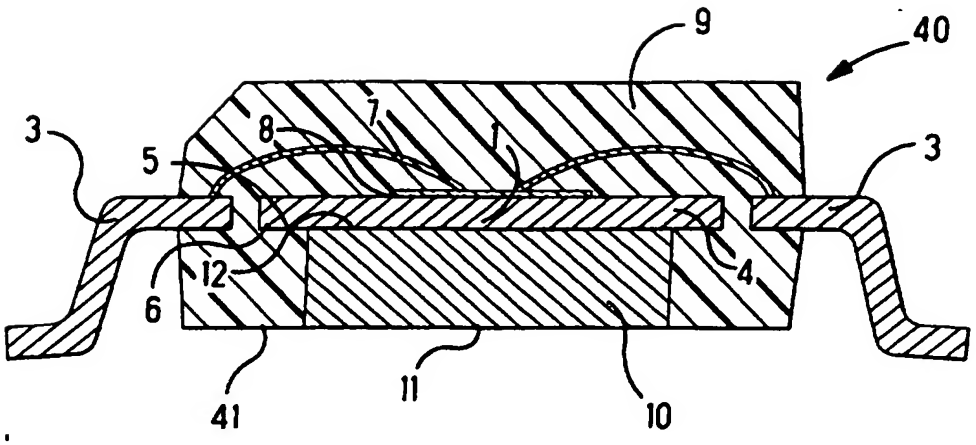

Fig. 1

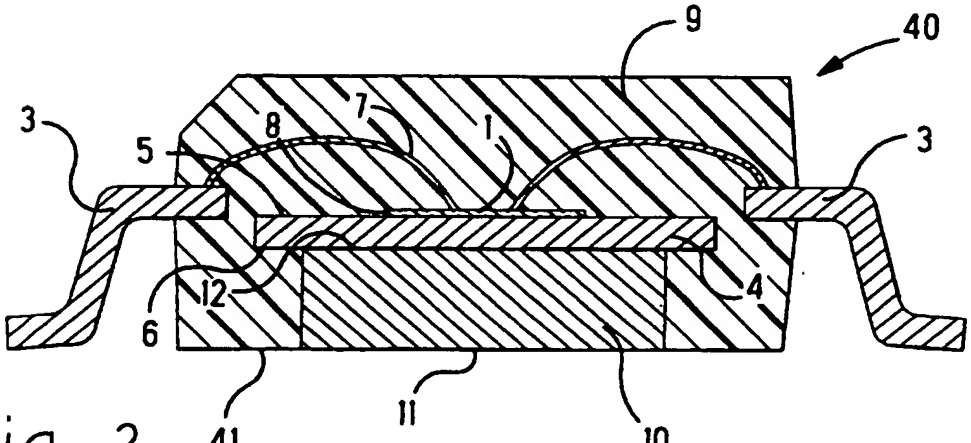

Fig. 2

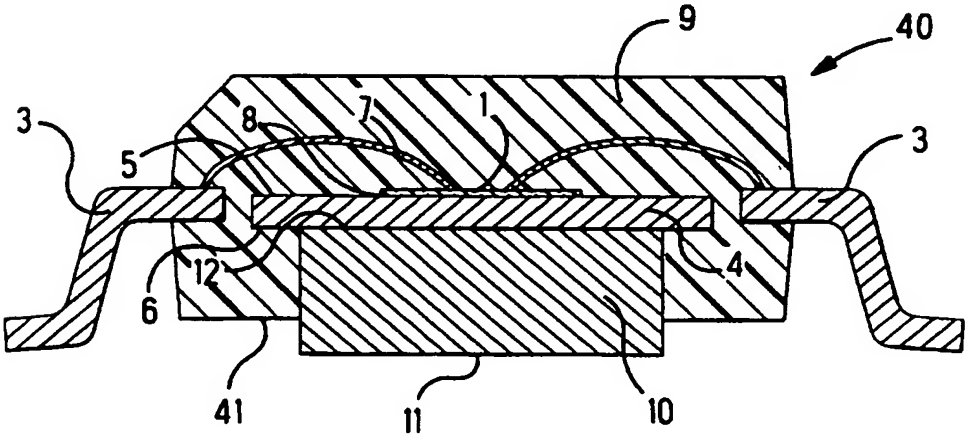

Fig. 3

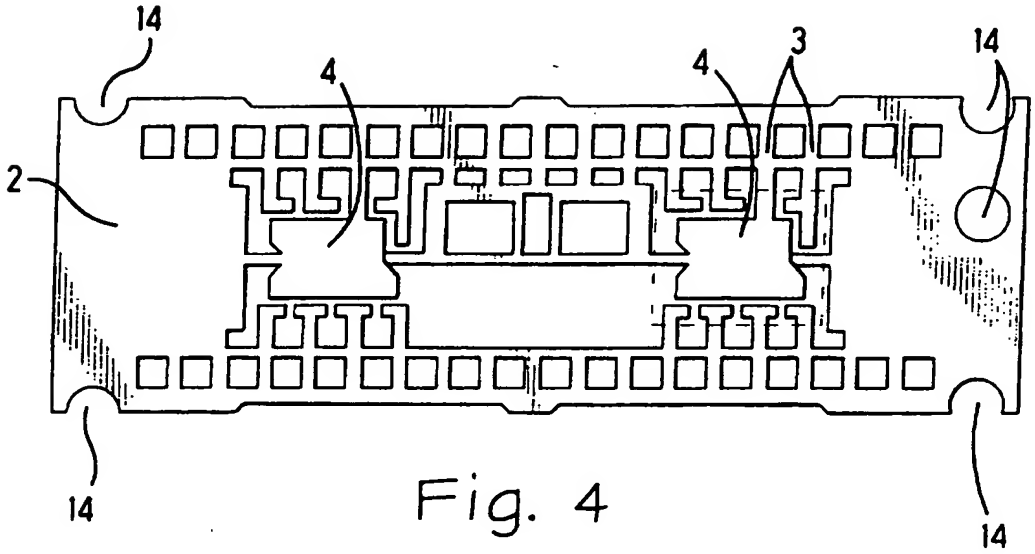

Fig. 4

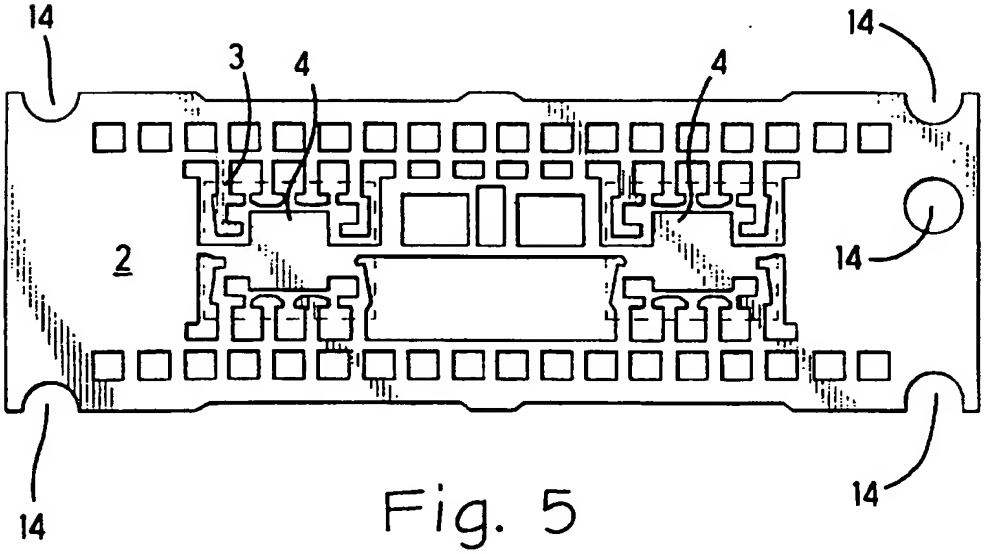

Fig. 5

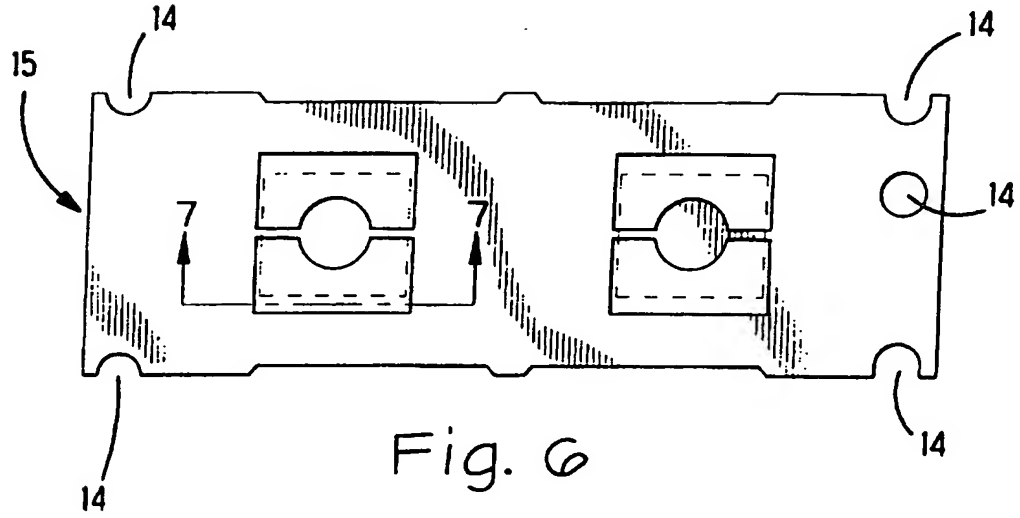

Fig. 6

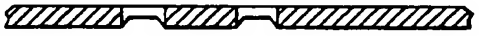

Fig. 7

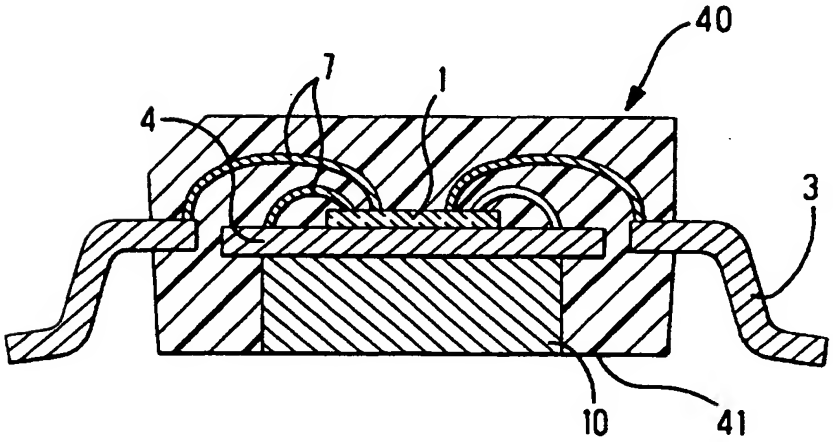

Fig. 8

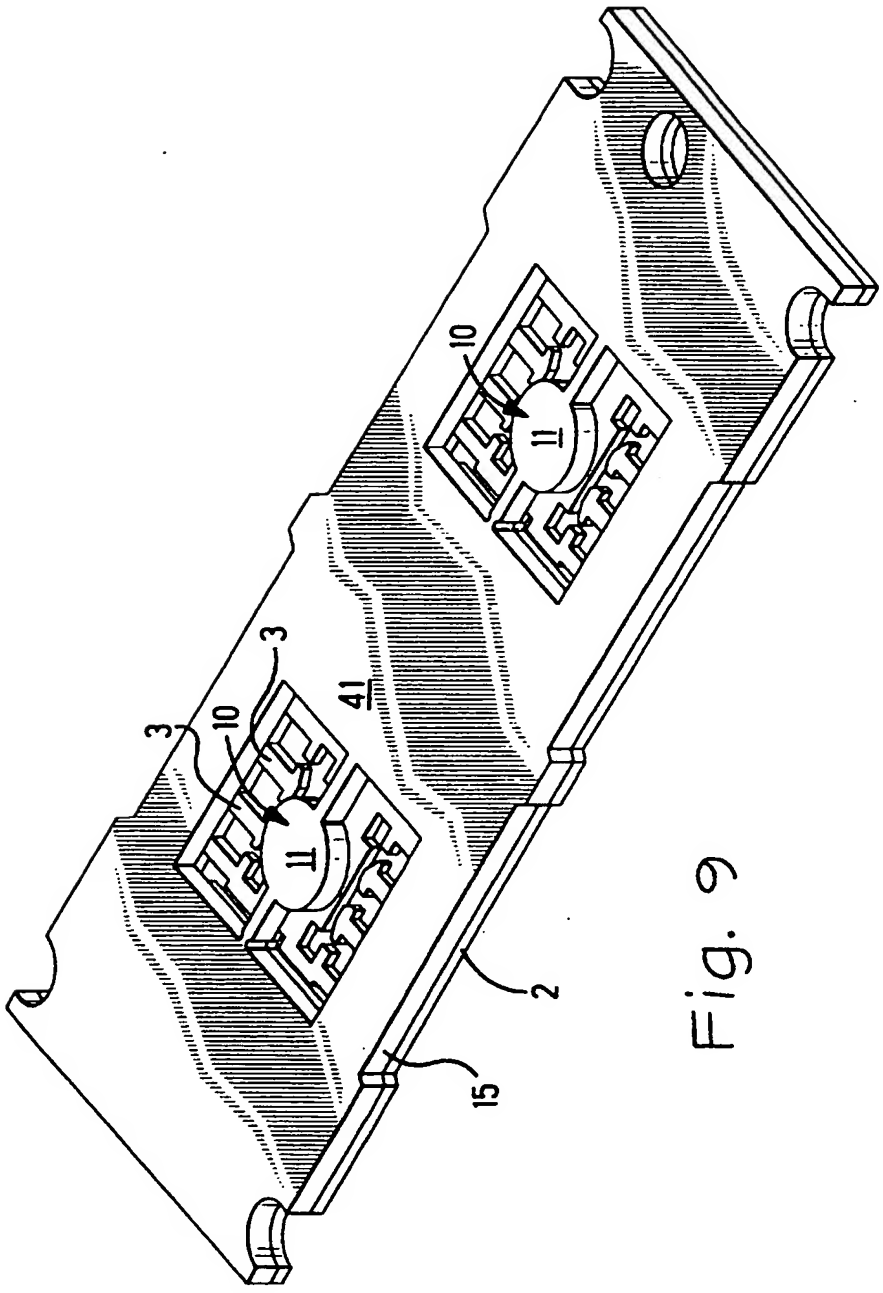

Fig. 6

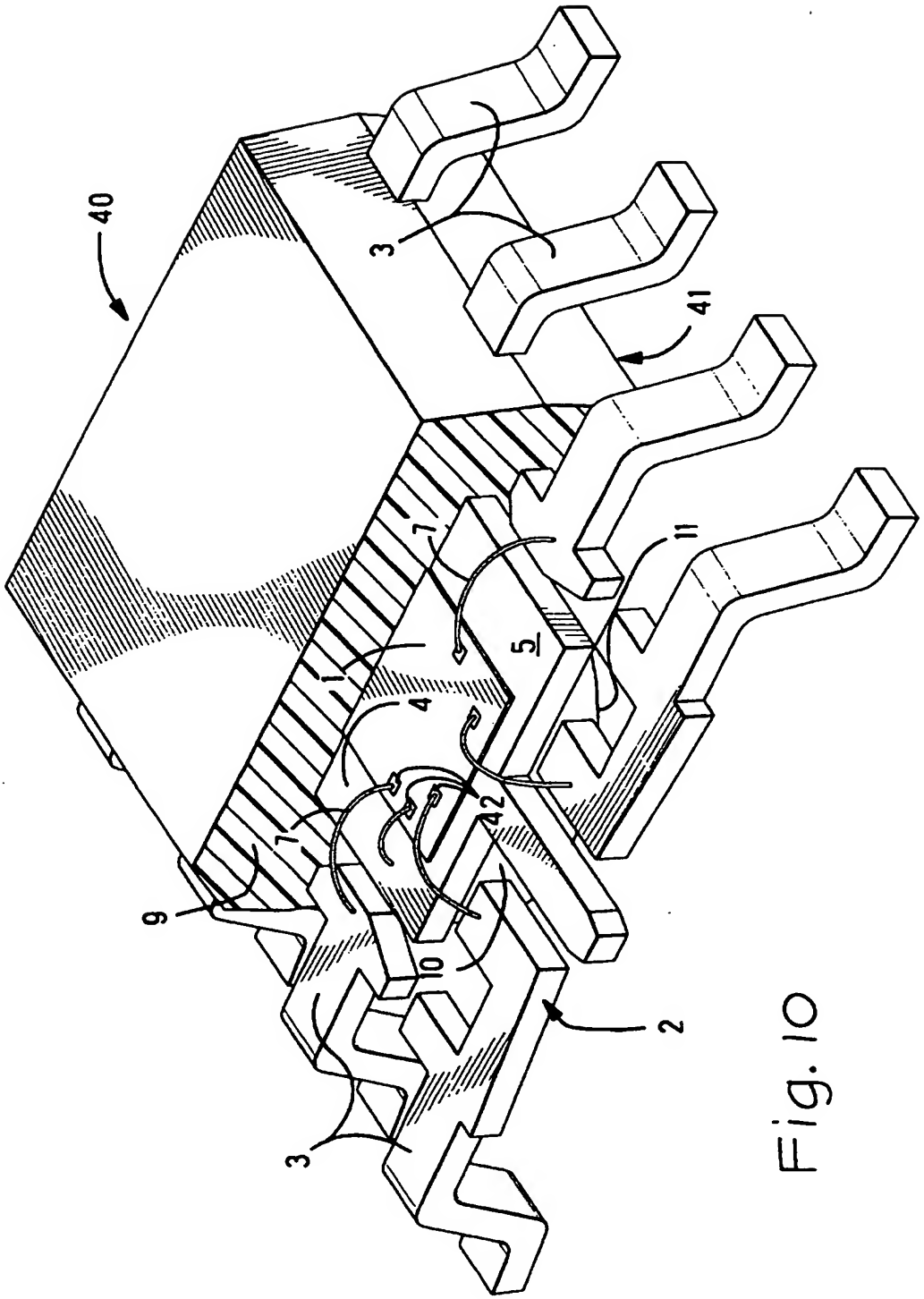

Fig. 10

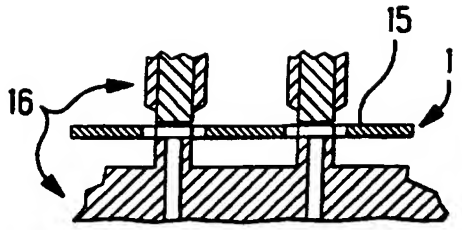

Fig. 11

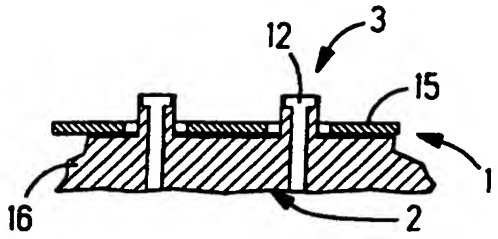

Fig. 12

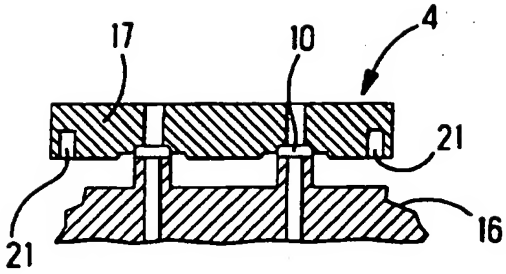

Fig. 13

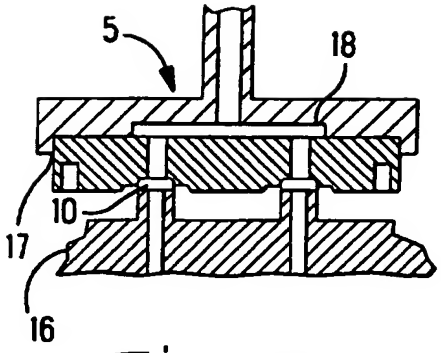

Fig. 14

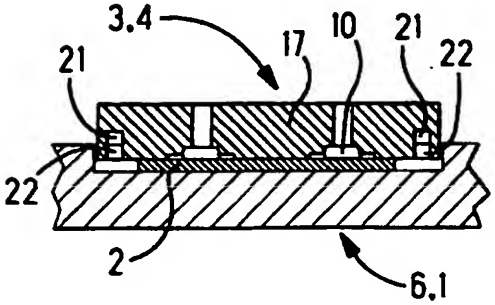

Fig. 15

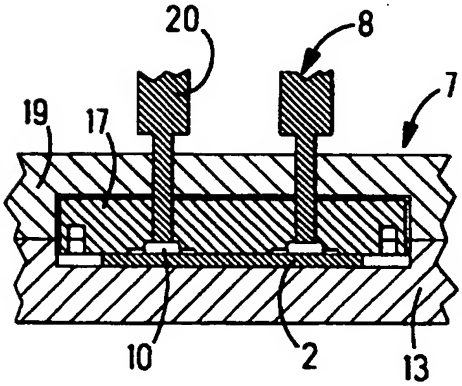

Fig. 16

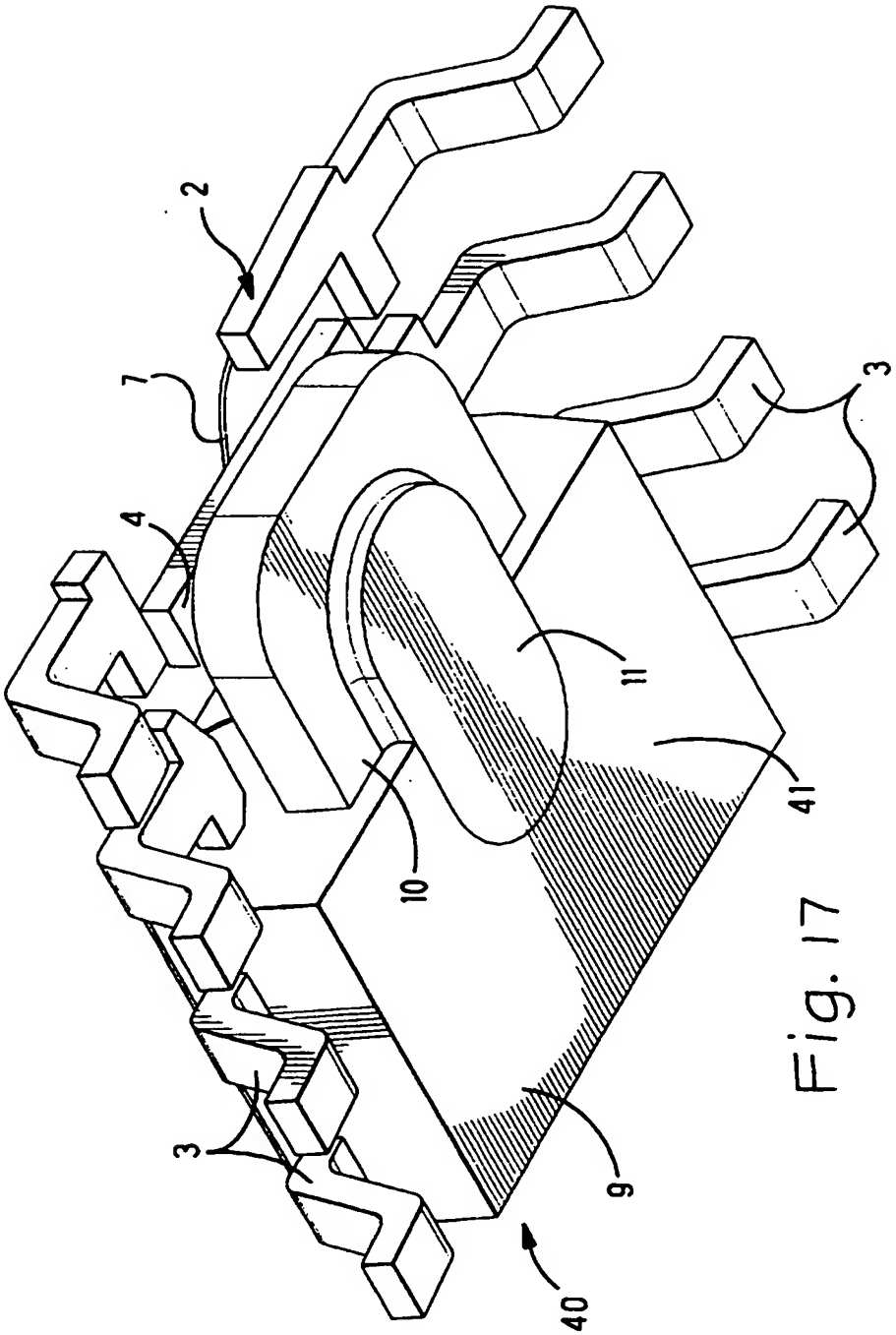

Fig. 17

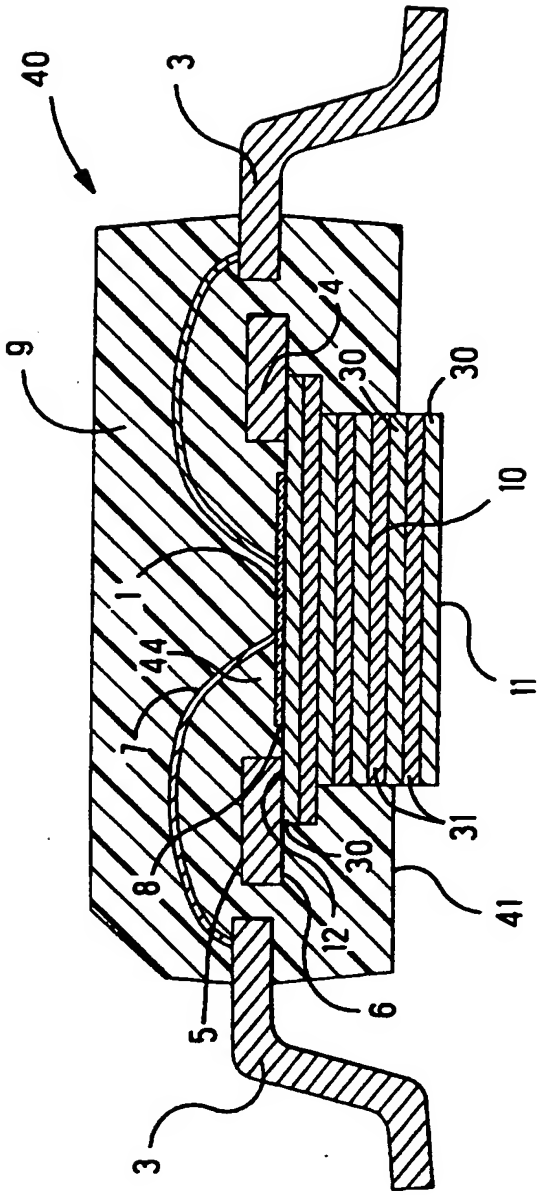

Fig. 18

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 97/01360

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/433

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 478 (E-1274), 5 October 1992 & JP 04 171749 A (MITSUBISHI ELECTRIC CORP), 18 June 1992, see abstract ---	1,3,4
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 402 (E-673), 25 October 1988 & JP 63 142838 A (MATSUSHITA ELECTRONICS CORP), 15 June 1988, see abstract --- -/--	1,2

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 May 1997	16. 06. 97
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Authorized officer Zeisler, P

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INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 97/01360

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 095, no. 009, 31 October 1995 & JP 07 153878 A (TOKYO TUNGSTEN CO LTD), 16 June 1995,	1,2,5,6, 12
A	see abstract & US 5 493 153 A (TADASHI ARIKAWA) 20 February 1996 see the whole document	13

X	EP 0 521 405 A (SUMITOMO ELECTRIC INDUSTRIES) 7 January 1993	1,4,5
A	see page 3, line 49 - page 4, line 5; figures 3,4 see page 8, line 43 - page 9, line 3	7,8,11

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INTERNATIONAL SEARCH REPORT

...ormation on patent family members

Intern... ...al Application No
PCT/US 97/01360

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		JP 5326767 A	10-12-93
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